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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981,021	10/16/2001	Frederic Boutaud	Analog.6202	5638

7590 11/04/2004

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EXAMINER	
SURYAWANSHI, SURESH	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Notice of Allowability	Application No.	Applicant(s)	
	09/981,021	BOUTAUD, FREDERIC	
	Examiner	Art Unit	
	Suresh K Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *application filed on 10/16/01*.

2. ☒ The allowed claim(s) is/are *1-17*.

3. ☒ The drawings filed on *16 October 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 9/22/03
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

The drawings filed on 10/16/01 are acceptable subject to correction of the informalities indicated below:

Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Reasons for Allowance

2. The following is an examiner's statement of reasons for allowance:

Cross (US Patent no 5,602,878[1]) discloses a method and apparatus for asynchronously transferring data from a first synchronous sequential logic circuit which derives its clock source from a first clock to a second synchronously sequential logic circuit which drives its clock source from a second clock, whereby metastability of the second synchronous sequential logic circuit is avoided. Cross does not disclose about a comparator and outputting the data on the data bus to the second device during the third, consecutive bus clock cycle when the sampled data is not equal to the data on the data bus during the second bus clock cycle.

Cole et al (US Patent no 6,260,152 B1) disclose a synchronization circuit that includes three flip-flops responsive to a common clock signal (CLK). The input to the first flip-flop represents the least significant bit (LSB) of a counter included within a first clock domain. The CLK signal originates from a second clock domain. The output of the first flip-flop is provided as input to the second flip-flop, while the second flip-flop output is provided as input to the third flip-flop and an exclusive OR (XOR) gate. In response to outputs from the second and third flip-flops, the XOR-gate produces a synchronization signal for use within the second clock domain. Cole et al do not disclose about a comparator and outputting the data on the data bus to the

[1] Cross is the prior art cited by applicant (dated 9/22/03).

second device during the third, consecutive bus clock cycle when the sampled data is not equal to the data on the data bus during the second bus clock cycle.

Nguyen (US Patent no 5,905,766) discloses a synchronizer for transferring data from a first clock domain having a first clock signal at a first clock rate to a second clock domain having a second clock signal at a second clock rate different from the first clock domain. The synchronizer includes a mechanism for transferring data from first clock domain to the second clock domain. Additionally, the synchronizer comprises a mechanism for synchronizing the transfer of data from the first clock domain to the second clock domain by the transferring mechanism. The synchronizer mechanism is self-timing based only on the first clock rate and second clock rate without any additional control signals. The synchronizing mechanism is connected with the transferring mechanism. Nguyen does not disclose about a comparator and outputting the data on the data bus to the second device during the third, consecutive bus clock cycle when the sampled data is not equal to the data on the data bus during the second bus clock cycle.

Larsen et al (US Patent no 6,715,095 B1) disclose a circuitry that receives data on an asynchronous communications bus from an external device and receives data from a synchronous internal device is provided. The circuitry, which preferably is an integrated circuit

chip, is capable of switching from synchronous operation to asynchronous operation without any loss of data. The circuitry comprises a register for receiving the data from the communications bus and for receiving the data from the internal device; event detection and synchronization logic for determining if there is activity on the communications bus and synchronizing such activity if detected during asynchronous operation; data capture and multiplexing logic for capturing data from the communications bus and transmitting the captured data to the register during synchronous operation; and clock switching logic. Larsen et al do not disclose about a comparator and outputting the data on the data bus to the second device during the third, consecutive bus clock cycle when the sampled data is not equal to the data on the data bus during the second bus clock cycle.

Dottling (JP 02183855 A) discloses a synchronous circuit synchronizes an asynchronous data effective signal with the clock cycle of a sensing chip to generate the first synchronous signal. The synchronous circuit further synchronizes the data effective signal with the clock cycle with a receiving chip to generate the second synchronous signal. The second synchronous signal is used to latch data loaded in the first register to the second latch in synchronous with the clock cycle, and the second register supplies data for successive processing under the control of the clock cycle of the receiving chip. With this, an asynchronous signal, which is generated in the chip having an on chip clocking system, which is different in speed, can be synchronized. Dattling does not disclose about a comparator and outputting the data on the data bus to the second device during the third, consecutive bus clock cycle when the sampled data is not equal

to the data on the data bus during the second bus clock cycle.

The prior art of record does not teach or suggest individually or in combination about a data register to sample data placed on a data bus by a first device during a first bus cycle and then a comparator to compare data on the data bus during a second, consecutive bus clock cycle to the data sampled by the data register and thereafter a multiplexor to output the sampled data to a second device during a third, consecutive bus cycle when the sampled data is equal to the data on the data bus during the second, consecutive bus clock cycle and to output data on the data bus to the second device during the third, consecutive bus clock cycle when the sampled data is not equal to the data on the data bus during the second bus clock cycle.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

3. Pursuant to MPEP 606.01, the title has been changed to read:

-- A CIRCUIT AND METHOD FOR PROVIDING CENTRALIZED SYNCHRONIZATION FOR THE TRANSPORTATION OF DATA BETWEEN DEVICES IN DIFFERENT CLOCK DOMAINS ON A DATA BUS --

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
October 28, 2004

Dennis M. Butler

Dennis M. Butler
Primary Examiner